Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **RG (2PADS)**
2. **V-IN**
3. **V+IN**
4. **V-**
5. **REF**
6. **V0**
7. **V+**
8. **RG (2PADS)**

**.080”**

**1**

**2**

**3**

**4**

**8**

**7**

**6**

**5**

**.141”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .080” X .141” DATE: 11/10/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 1NA121**

**DG 10.1.2**

#### Rev B, 7/1